Attorney Docket No. 251173USUS2CONT

Inventor: Tadashi MATSUDA

Preliminary Amendment

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IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): An insulated gate bipolar transistor comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type formed on a top surface

of said first semiconductor layer;

a base layer of the first conductivity type formed on a top surface of said second

semiconductor layer;

a plurality of gate electrodes each of which is buried in a trench with a gate insulation

film interposed therebetween, said trench being formed in said base layer to a depth reaching

said second semiconductor layer from a surface of said base layer, each said gate electrode

having an upper surface of a rectangular pattern with different widths in two orthogonal

directions, said gate electrodes being disposed in a direction along a short side of the

rectangular pattern;

emitter layers of the second conductivity type formed in the surface of said base layer

to oppose both end portions of each said gate electrode in a direction along a long side of the

rectangular pattern;

a first main electrode in contact with said emitter layers and said base layer; and

a second main electrode formed at a bottom surface of said first semiconductor layer.

Claim 2 (Original): The transistor according to claim 1, wherein said emitter layers

are formed as impurity diffusion layers opposing three side faces at the both end portions of

each said gate electrodes in the long side direction.

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Claim 3 (Original): The transistor according to claim 2, wherein said emitter layers

are impurity diffusion layers formed independently of each other at the both end portions of

each said gate electrode in the long side direction.

Claim 4 (Currently Amended): The transistor according to claim 2, wherein said

emitter layers are impurity diffusion layers continuously formed to extend and overlie

between said plurality of gate electrodes while opposing the both end portions of each said

gate electrode in the long-side direction isolated trench gates aligned in the short side

direction thereof.

Claim 5 (Original): The transistor according to claim 2, wherein said gate electrodes

include multiple ones aligned in the long side direction also, and wherein said emitter layers

are impurity diffusion layers formed to continue between two neighboring gate electrodes

while opposing respective end portions of said two neighboring gate electrodes in the long

side direction.

Claims 6-13 (Canceled).

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